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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,522	03/17/2004	Valeriy Sukharev	02-6392/1D	3975
24319	7590	11/03/2005	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035			DIAZ, JOSE R	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/802,522

Applicant(s)

SUKHAREV ET AL.

Examiner

José R. Díaz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 August 2005.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 18-25 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 18-25 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 18-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Sinha et al. (US 2003/0227091 A1).

Regarding claim 18, Sinha et al. teaches an integrated circuit, the improvement comprising a metal interconnect including:

a copper layer (30) formed between dielectric structures (20), where the dielectric structures have an upper level (consider the upper surface in contact with layer 25), where the upper level of the dielectric structures is substantially uniform across all of the dielectric structures (20) [see fig. 8B],

the copper layer (30) planarized to be below the upper level of the dielectric structures (consider the interface between layers 20 and 25), the copper layer having no dishing between the dielectric structures (please note that the upper surface of the planarized copper layer 30 is uniform and smooth indicating that no dishing is formed on the upper surface) [see fig. 8B], and

an electrically conductive capping layer (43) over all of the copper layer, with

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none of the capping layer over any of the dielectric structures (20) [see fig. 8B].

Regarding claim 19, Sinha et al. further teaches that the capping layer (43) is at least partially above the upper level of the dielectric structures (compare the upper surface of layer 43 with the upper surface of layer 20) [see fig. 8B].

Regarding claim 20, Sinha et al. further teaches that the electrically conductive capping layer (43) comprises an alloy of at least one of cobalt and nickel [see paragraph 0030].

Regarding claim 21, Sinha et al. teaches a copper layer (30) formed by electrochemical deposition [see paragraph 0030].

Regarding claim 22, Sinha et al. teaches a copper layer (30) planarized by any suitable method [see paragraph 0029].

Regarding claim 23, Sinha et al. teaches that the electrically conductive capping layer comprises a material formed by electroless deposition [see paragraph 0030].

Regarding claim 24, Sinha et al. teaches that the dielectric structures (20) comprise low k materials (TEOS) [see paragraph 0024].

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sinha et al. (US 2003/0227091 A1) in view of Ueno et al. (US 2004/0126548 A1).

Regarding claim 15, Sinha et al. fails to teach an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures. However, Ueno et al. teaches that it is well known in the art to include an inter metallic dielectric layer (13) over the electrically conductive capping layer (29) and the dielectric structures (13) [see fig. 4].

Sinha et al. and Ueno et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures. The motivation for doing so is increasing the density of integrated circuit structures. Therefore, it would have been obvious to combine Ueno et al. with Sinha et al. to obtain the invention of claim 25.

### ***Response to Arguments***

5. Applicant's arguments with respect to claims 18-25 have been considered but are moot in view of the new grounds of rejection.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Toyoda et al. (US 2004/0005774 A1) teaches a copper layer (103) and a capping layer (104) between structures (101) [see figs. 3A-3B].

7. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

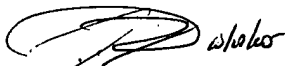
### ***Correspondence***

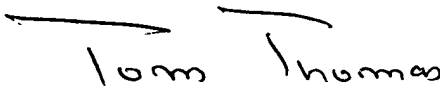
Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
José R. Díaz  
Examiner  
Art Unit 2815

  
TOM THOMAS  
SUPERVISORY PATENT EXAMINER